## JVL

## SERVICE MANUAL AUDIONIDEO CONTROL RECEIVER

## RX-7001PGD



## Contents

Safety precautions ..... 1-2
Disassembly method ..... 1-3
Adjustment method ..... 1-9
Description of major ICs ..... 1-10

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by ( 1 ) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)

After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
Do not use a line isolation transformer during this check.

- Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5 mA AC (r.m.s.)
- Alternate check method

Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a $1,500 \Omega 10 \mathrm{~W}$ resistor paralleled by a $0.15 \mu \mathrm{~F}$ AC-type capacitor between an exposed metal part and a known good earth ground.
Measure the AC voltage across the resistor with the AC voltmeter.
Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to $0.5 \mathrm{~mA} A C$ (r.m.s.).


## Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

## CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

## Disassembly method <br> ■Removing the top cover (See Fig.1)

1. Remove the four screws $A$ attaching the top cover on both sides of the body.
2. Remove the three screws $B$ on the back of the body.
3. Remove the top cover from behind in the direction of the arrow while pulling both sides outward.

## ■Removing the front panel assembly

(See Fig. 2 and 3)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from connector CN400 on the main board and CN402 on the power supply board in the front panel assembly.
2. Cut off the tie band fixing the harness.
3. Disconnect the harness from connector CN202 on the video board.
4. Remove the three screws $C$ attaching the front panel assembly.
5. Remove the five screws $D$ attaching the front panel assembly on the bottom of the body. Detach the front panel assembly toward the front.

## ■Removing the rear panel (See Fig.4)

- Prior to performing the following procedure, remove the top cover.

1. Remove the power cord stopper from the rear panel by moving it in the direction of the arrow.
2. Remove the twenty-eight screws $E$ attaching the each boards to the rear panel on the back of the body.
3. Remove the three screws $F$ attaching the rear panel on the back of the body.


Fig. 2


Fig. 3


Fig. 4

## ■Removing each board connected to the rear side of the main board

(See Fig. 5 to 9)

- Prior to performing the following procedure, remove the top cover and the rear panel.

1. Cut off the tie band fixing the harness.
2. Disconnect the harness from connector CN2O2 on the video board.
3. Disconnect the tuner board from connector CN101 on the main board.
4. Disconnect the SEA board and the audio board from connector CN452, CN301and CN302 on the main board.
5. Disconnect the V-audio board from connector CN303 on the main board.
6. Disconnect the relay board 4.Then, disconnect the video board and the S -video board from connector CN201 and CN241 on the main board.
7. Disconnect the DSP board from connector CN501 and CN601 on the main board while removing the DSP board from the bracket fixing the lower part of the DSP board at the same time.
8. Disconnect the compulink board from connector CN255 on the main board.

Compulink board


Fig. 9


Fig. 5


Fig. 6


Fig. 7


Fig. 8

## ■Removing the main board / regulator board (See Fig. 10 to 12)

- Prior to performing the following procedure, remove the top cover and the rear panel.

ATTENTION: It is not necessary to remove the boards connected to the back of the main board. But to disassemble the main board and the power supply board efficiently, remove them.

1. Disconnect the card wire from connector CN400 on the main board.
2. Cut off the three tie bands fixing the harnesses.
3. Disconnect the harness from connector CN811 on the power transformer board.
4. Disconnect the relay board 1,2 and 3 from the main board and the power supply board.
5. Disconnect the harness from connector CN704, CN821, CN901, CN711, CN712, CN931 and CN932.
6. Remove the screw $G$ attaching the regulator board to the heat sink cover.
7. Remove the four screws H attaching the main board to the heat sink cover.
8. Remove the five screws I and the screw J attaching the main board to the chassis base (The resistor board will come off at the same time).

## $■$ Removing the resistor board (See Fig.13)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the harness from connector CN881 on the resistor board.
2. Remove the screw J attaching the resistor board.


Fig. 10


Fig. 11 Regulator board


Fig. 12


Fig. 13

## - Removing the amplifier board

(See Fig. 10 and 14)

- Prior to performing the following procedure, remove the top cover.

1. Cut off the four tie bands fixing the harnesses.
2. Disconnect the harnesses from connector CN711, CN712, CN704 and CN901 on the main board respectively.
3. Disconnect the harnesses from connector CN953 on the SP terminal board.
4. Remove the four screws $K$ and six screws $L$ attaching the amplifier board.

## - Removing the power transformer

(See Fig.15)

- Prior to performing the following procedures, remove the top cover.

1. Unsolder the seven harnesses connected to the power transformer.
2. Disconnect the harness from connector CN811 and the harnesses connected to connector CN55 and CN56 on the power transformer board.
3. Remove the four screws $M$ attaching the power transformer.

## ■Removing the Voltage selector board

(See Fig.16)

- Prior to performing the following procedure, remove the top cover and the rear panel.

1. Unsolder the six harnesses connected to the Voltage selector board.

## ■ Removing the power / fuse board

(See Fig.17)

- Prior to performing the following procedure, remove the top cover and the rear panel.

1. Remove the screw N attaching the power / fuse board.
2. Unsolder the power cord and other harnesses connected to the power / fuse board.


Fig. 10


Fig. 14


Fig. 15


Fig. 16


Fig. 17

## -Removing the power supply board

 (See Fig. 18 and 19)- Prior to performing the following procedure, remove the top cover and the front panel.

1. Remove the one nut attaching the headphone jack of the power supply board on the front side of the body.
2. Disconnect the relay board 1, 2 and 3 from the power supply board and the main board respectively.
3. Disconnect the harness connected to connector CN55 and CN56 on the power transformer board (If necessary, cut off the band fixing the harness on the side of the base chassis).
4. Remove the four screws $O$ attaching the power supply board and pull out the power supply board from the front bracket backward.
5. Unsolder the three harnesses connected to the power supply board.

## ■Removing the system control board / power switch board (See Fig. 20 to 21)

- Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Pull out the volume knob on the front side of the front panel and remove the nut attaching the system control board.
2. Remove the six screws $P$ attaching the system control board on the back of the front panel and disconnect the harness from connector CN422 on the system control board.
3. Disconnect the harness from connector CN430 on the power switch board.
4. Remove the five screws $Q$ attaching the power switch board.


Fig. 18


Fig. 19


Fig. 20


Fig. 21

Removing the operation switch board
(See Fig. 22 to 24)

- Prior to performing the following procedure, remove the top cover, the front panel assembly and the system control board.

1. Remove the six screws $R$ attaching the operation switch board on the back of the front panel.
2. On the back of the front panel, release the four joints by pushing the joint tabs inward. Remove the operation switch board toward the front.
3. Pull out the multi jog knob and the source selector knob.
4. Remove the two screws $S$ attaching the operation switch board.


Fig. 22


Fig. 23


Fig. 24

## Adjustment method

## $\square$ Tuner section

1.Tuner range

| FM | $87.5 \mathrm{MHz} \sim 108.0 \mathrm{MHz}$ |
| :--- | :--- |
| AM(MW) | $530 \mathrm{kHz} \sim 1710 \mathrm{kHz}$ |

## Power amplifier section

## Adjustment of idling current

Measurement location
Adjustment part

TP781
VR787(Lch) , VR788(Rch)

## Attention

This adjustment does not obtain a correct adjustment value immediately after the amplifier is used (state that an internal temperature has risen).
Please adjust immediately after using the amplifier after turning off the power supply of the amplifier and falling an internal temperature.
<Adjustment method>
1.Set the volume control to minimum during this adjustment.(No signal \& No load)
2. Set the surround mode OFF.
2.Turn VR787 and VR788 fully counterclockwise to warm up before adjustment. If the heat sink is already warm from previous use the correct adjustment can not be made.
3.For L-ch,connect a DC voltmeter between TP781's pin1 and pin2 (Lch)

And,connect it between pin3 and pin4(Rch).
4.30 minutes later after power on, adjust VR787 for L-ch, or VR788 for R-ch so that the DC voltmeter value has $1 \mathrm{mV} \sim 10 \mathrm{mV}$.

* It is not abnormal though the idling current might not become 0 mA even if it is finished to turn variable resistance (VR787,VR788) in the direction of counterclockwise.



## Description of major ICs

## AK4527 (IC601) : A/D,D/A Converter

1.Pin layout

2.Block diagram


Block Diagram (DIR and AC-3) DSP are external parts)

| 3. Pin function (1/2) |
| :--- |
| No. |
| Pin name |
| $1 /$ I/ |
| 1 | SDOS $\quad$ I | SDTO Source select pin |
| :--- |
| "L" : Internal ADC output, "H" : DAUX input |
| ORed with serial control register if P/S="L". |

3.Pin function (2/2)

| No. | Pin Name | I/O | Function |
| :---: | :--- | :---: | :--- |
| 33 | VREFL | I | Negative voltage reference Input pin, AVSS |
| 34 | VCOM | O | Common voltage output pin,AVDD/2 <br> Large external capacitor around 2.2 LuF is used to reduce power-supply noise |
| 35 | VREFH | I | Positive voltage reference input pin,AVDD |
| 36 | AVDD | - | Analog power supply pin |
| 37 | AVSS | - | Analog ground pin |
| 38 | XTI | I | X'tal input pin |

■ BA15218F(IC303):OP AMP.


## BA15218N (IC501, IC510, IC511) : Dual Ope. Amp.



## BA7625 (IC242,IC201) / BA7626 (IC241): Video selector



| A | $B$ | $E$ | MONITOR OUT |
| :---: | :---: | :---: | :---: |
| $L$ | $L$ | $*$ | IN1 |
| $H$ | $L$ | $*$ | IN2 |
| $L$ | $H$ | $*$ | IN3 |
| $H$ | $H$ | $L$ | IN4 |
| $H$ | $H$ | $H$ | IN5 |


| C | D | $E$ | VOUT1 |
| :---: | :---: | :---: | :---: |
| $L$ | $L$ | $*$ | -- |
| $H$ | $L$ | $*$ | IN2 |
| $L$ | $H$ | $*$ | IN3 |
| $H$ | $H$ | $L$ | IN4 |
| $H$ | $H$ | $H$ | IN5 |


| C | D | E | VOUT2 |
| :---: | :---: | :---: | :---: |
| L | L | $*$ | IN1 |
| $H$ | L | $*$ | -- |
| L | $H$ | $*$ | IN3 |
| $H$ | $H$ | L | IN4 |
| $H$ | $H$ | $H$ | IN5 |

## BU2092(IC402,IC405):LED Controller


2.Pin Function

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | Vss | - | Connect to GND |
| 2 | DATA | 1 | Serial Data input |
| 3 | CLOCK | 1 | Shift Clock of Data |
| 4 | LCK | 1 | Latch Clock of Data |
| 5~16 | Q0~Q11 | O | Parallel Data Output |
| 17 | OE | 1 | Output Enable |
| 18 | Vdd | - | Power Supply |

## BU4066BCF (IC602,IC611) : Switch

## 1.Pin Layout



## 2.Block Diagram



■W24L011AJ-15(IC641):SDRAM

| 1.Pin layout |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| A0 | 1 | 32 | A16 |
| A1 | 2 | 31 | A15 |
| A2 | 3 | 30 | A14 |
| A3 | 4 | 29 | A13 |
| CS | 5 | 28 | OE |
| I/O1 | 6 | 27 | 1/08 |
| I/O2 | 7 | 26 | 1/07 |
| VDD | 8 | 25 | VSS |
| VSS | 9 | 24 | VDD |
| I/O3 | 10 | 23 | I/O6 |
| I/O4 | 11 | 22 | I/O5 |
| WE | 12 | 21 | A12 |
| A4 | 13 | 20 | A11 |
| A5 | 14 | 19 | A10 |
| A6 | 15 | 18 | A9 |
| A7 | 16 | 17 | A8 |

2.Block diagram

3.Pin function

| Symbol | Description |
| :---: | :--- |
| A0~A16 | Address inputs |
| $\mathrm{I} / \mathrm{O} 1 \sim \mathrm{I} / \mathrm{O} 8$ | Data inputs/outputs |
| CS | Chip select inputs |
| WE | Write enable input |
| OE | Output enable input |
| Vdd | Power supply |
| Vss | Ground |

■ LA1838(IC102): FM AM IF AMP\&detector, FM MPX Decoder

1. Block Diagram

2. Pin Function

| Pin No. | Symbol | 1/0 | Function | $\begin{array}{\|l\|} \hline \text { Pin } \\ \text { No. } \\ \hline \end{array}$ | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | FM IN | 1 | This is an input terminal of FM IF signal. | 16 | R OUT | 0 | Right channel signal output. |
| 2 | AM MIX | 0 | This is an out put terminal for AM mixer. | 17 | L OUT | O | Left channel signal output. |
| 3 | FM IF | 1 | Bypass of FM IF | 18 | R IN | 1 | Input terminal of the Right channel post AMP. |
| 4 | AM IF | 1 | Input of AM IF Signal. | 19 | L IN | 1 | Input terminal of the Left channel post AMP. |
| 5 | GND | - | This is the device ground terminal. | 20 | RO | $\bigcirc$ | Mpx Right channel signal output. |
| 6 | TUNED | O | When the set is tunning,this terminal becomes "L". | 21 | LO | O | Mpx Left channel signal output. |
| 7 | STEREO | O | Stereo indicator output. Stereo "L", <br> Mono: "H" | 22 | IF IN | I | Mpx input terminal |
| 8 | VCC | - | This is the power supply terminal. | 23 | FM OUT | 0 | FM detection output. |
| 9 | FM DET | - | FM detect transformer. | 24 | AM DET | 0 | AM detection output. |
| 10 | AM SD | - | This is a terminal of AM ceramic filter. | 25 | AM AGC | 1 | This is an AGC voltage input terminal for AM |
| 11 | FM VSM | 0 | Adjust FM SD sensitivity. | 26 | AFC | - | This is an output terminal of voltage for FM-AFC. |
| 12 | AM VSM | O | Adjust AM SD sensitivity. | 27 | AM RF | 1 | AM RF signal input. |
| 13 | MUTE | I/O | When the signal of IF REQ of IC121( LC72131) appear, the signal of FM/AM IF output. //Muting control input. | 28 | REG | O | Register value between pin 26 and pin28 besides the frequency width of the input signal. |
| 14 | FM/AM | 1 | Change over the FM/AM input. <br> "H" :FM, "L" : AM | 29 | AM OSC | - | This is a terminal of AM Local oscillation circuit. |
| 15 | MONO/ST | 0 | Stereo : "H", Mono: "L" | 30 | OSC BUFFEP | O | AM Local oscillation Signal output. |

## ■ LC72136N (IC121) : PLL Frequency synthesizer

1. Pin layout

| XT | 1 | $\bigcirc 22$ | XT |
| :---: | :---: | :---: | :---: |
| FM/AM | 2 | 21 | GND |
| CE | 3 | 20 | LPFOUT |
| DI | 4 | 19 | LPFIN |
| CLOCK | 5 | 18 | PD |
| DO | 6 | 17 | VCC |
| FM/ST/VCO | 7 | 16 | FMIN |
| AM/FM | 8 | 15 | AMIN |
|  | 9 | 14 |  |
|  | 10 | 13 | IFCONT |
| SDIN | 11 | 12 | IFIN |

## 2. Block diagram


3. Pin function

| Pin <br> No. | Symbol | I/O | Function | Pin <br> No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :--- | :---: | :---: | :---: | :--- |
| 1 | XT | I | X'tal oscillator connect $(75 \mathrm{kHz})$ | 12 | IFIN | I | IF counter signal input |
| 2 | $\overline{\text { FM/AM }}$ | O | LOW:FM mode | 13 | IFCONT | O | IF signal output |
| 3 | CE | I | When data output/input for 4pin(input) and <br> 6pin(output): H | 14 |  | - | Not use |
| 4 | DI | I | Input for receive the serial data from <br> controller | 15 | AMIN | I | AM Local OSC signal output |
| 5 | CLOCK | I | Sync signal input use | 16 | FMIN | I | FM Local OSC signal input |
| 6 | DO | O | Data output for Controller <br> Output port | 17 | VCC | - | Power suplly (VDD=4.5-5.5V) <br> When power ON:Reset circuit move |
| 7 | FM/ST/VCO | O | "Low": MW mode | 18 | PD | O | PLL charge pump output(H: Local OSC <br> frequency Height than Reference frequency. |
| 8 | $\overline{\text { AM/FM }}$ | O | Open state after the power on reset | 19 | LPFIN | I | Input for active lowpassfilter of PLL |
| 9 | LW | I/O | Input/output port | 20 | LPFOUT | O | Output for active lowpassfilter of PLL |
| 10 | MW | I/O | Input/output port | 21 | GND | - | Connected to GND |
| 11 | SDIN | I/O | Data input/output | 22 | $\overline{\text { XT }}$ | I | X'tal oscillator(75KHz) |

## LC7522 (IC451) : SEA Control

1.Pin layout
2.Block diagram


3. Pin function

| Pin No. | Symbol | Function |
| :---: | :---: | :---: |
| 1 | Vod | Power Supply terminal for Audio signal +7 V (typ) |
| 18 | Vss | Power Supply terminal OV |
| 14 | Vee | Power Supply terminal for Audio signal. Single channel use, joint VSS. |
| 15 | Vcc | Power Supply terminal +5 V (typ) |
| 2,27 | IN 1 | Audio signal Input terminal |
| 3,26 | IN 2 | IN1 joint opposite input of Operation amp. |
|  |  | IN2 joint inapposite input of Operation amp. |
|  |  | It have Right and Left. |
| 16 | D1 | Data input terminal from CPU Shumit inverter style |
| 17 | CLK | Clock input terminal from CPU |
| 4~10 | f1~7 | Joint terminal of B.P.F. |
| 19~25 |  | f1~f7 X Right, Left Total 14 terminal |
| 11 | TEST1 | Internal test terminal of IC |
| 12 | TEST2 | It can use open condition |
| 13 | S | Select terminal for 2 tip use |
|  |  | "1" input, key code 7C3 - VDD joint |
|  |  | "0" input, key code 7C2 - VEE joint |
| 28 | NC | No use |

## M5243AP12(IC452):S.E.A.Graphic equalizer



## NJM4580D (IC301, IC302, IC306) : LPF, Mic and H.phone Amp.

1.Terminal layout

2.Block diagram


## MN101C15FDE (IC401) : System control micon

## 1. Pin layout


2. Pin function

| Pin <br> No | Symbol | Functions | \|rin | Symbol | Functions |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | GND | Ground | 41 | VIDEO3 | VIDEO 3 signal terminal |
| 2 | DVD-S/C | DVD S/C signal select terminal | 42 | VIDEO4 | VIDEO 4 signal terminal |
| 3 | VCR1-S/C | VCR1 S/C signal select terminal | 43 | S.MUTE | Source mute control terminal |
| 4 | VIDEO-S/C | VIDEO S/C signal select terminal | 44 |  | No use |
| 5 | TV-S/C | TV S/C select terminal | 45 |  | No use |
| 6 | 4/8-IN | 4 ohm / 8 ohm select signal terminal | 46 |  | No use |
| 7 |  |  | 47 | RDS-DATA | RDS control signal terminal |
| 8 | GND | Ground | 48 |  | No use |
| 9 | PROTECT | Protect | 49 | RDS-CLK | RDS control signal clock |
| 10 | GND | Ground | 50 | DSP-READY | DSP control signal clock |
| 11 | VDD | Power supply | 51 | DSP-RESET | DSP reset signal terminal |
| 12 | OSC 12 | Oscillation terminal | 52 | M/CS | Control signal from IC400 |
| 13 | OSC 11 | Oscillation terminal | 53 | M-RESET | Reset signal from IC400 |
| 14 | VSS | Ground | 54 | M-STATUS | Status signal from IC400 |
| 15 | X1 | Ground | 55 | M-COMMAND | Command signal from IC400 |
| 16 | X0 | Ground | 56 | M-CLK | Clock signal from IC400 |
| 17 | GND | Ground | 57 | SEA-CLK | SEA clock signal from terminal |
| 18 | TEXT-OUT | Text signal output terminal | 58 | SEA-DATA | SEA data signal terminal |
| 19 | TEXT-IN | Text signal input terminal | 59 | VL/VH | Connect to power supply board |
| 20 | MASTER | Master signal terminal | 60 | 4/8 OUT | $4 \mathrm{ohm} / 8$ ohm select signal terminal |
| 21 | DSP-COMMAND | DSP control signal terminal | 61 | SW-DATA | Switch data signal terminal |
| 22 | DSP-STATUS | DSP control signal terminal | 62 | SW-CLK | Switch clock signal terminal |
| 23 | DSP-CLK | DSP control signal terminal | 63 | VOL-STB | Volume strobe signal terminal |
| 24 |  | No use | 64 | VOL-DATA | Volume data signal terminal |
| 25 | RESET-IN | Reset signal input terminal | 65 | VOL-CLK | Volume clock signal terminal |
| 26 | TUNER-CE | Tuner chip enable | 66 | SW-STB | Switch strobe signal terminal |
| 27 | TUNER-CLK | Tuner clock signal terminal | 67 |  | No use |
| 28 |  | No use | 68 |  | No use |
| 29 | TUNER-DATA | Tuner control signal terminal | 69 | FR1-RELAY | Relay 1 signal terminal |
| 30 | TUNER-MUTE | Tuner mute signal terminal | 70 | FR2-RELAY | Relay 2 signal terminal |
| 31 | TUNER-IN | Tuner signal input terminal | 71 | CNTR-RELAY | Center speaker relay terminal |
| 32 | STEREO-IN | Stereo signal input terminal | 72 | SUR-RELAY | Surround speaker relay terminal |
| 33 | RDS-ST | No use | 73 | SUB-MUTE | SUB woofer out mute control |
| 34 | M-BUSY | Busy signal from IC400 | 74 | LED-LCK2 | LED latch clock signal terminal |
| 35 | INH | No use | 75 | C.TONE3 | Center tone 3 signal terminal |
| 36 | OSD-DATA | OSD data signal input terminal | 76 | C.TONE2 | Center tone 2 signal terminal |
| 37 | OSD-STB | OSD standby signal terminal | 77 | C.TONE1 | Center tone 1 signal terminal |
| 38 | OSD-CLK | OSD clock signal terminal | 78 | LED-LCK1 | LED latch clock signal terminal |
| 39 | VIDEO1 | VIDEO 1 signal terminal | 79 | LED-DATA | LED data signal terminal |
| 40 | VIDEO2 | VIDEO 2 signal terminal | 80 | LED-CLK | LED clock signal terminal |

## MN173222DG(IC400):FL Display \& Operation switch control

1.Pin layout

| 1 | $84 \sim 64$ |
| :---: | :---: |
| 2 | 63 |
| 21 |  |
| $22 \sim 42$ |  |

2.Key matrix

|  | KEY OUT 0 | KEY OUT1 | KEY OUT 2 | KEY OUT 3 | KEY OUT 5 |
| :--- | :---: | :---: | :---: | :---: | :---: |
| KEY IN 0 | POWER | ANALOG/ <br> DIGITAL | SEA ADJUST | FM/AM TUNING | ONE TOUCH <br> OPERATION |
| KEY IN 1 | SURROUND | DSP MODE | FM MODE | TUNER PRESET | - |
| KEY IN 2 | SPEAKER 1 | LOUDNESS | LEVEL ADJUST | MEMORY | - |
| KEY IN 3 | SPEAKER 2 | SEA MODE | SOUND SELECT | SETTING | - |

3.Pin function

| Pin No. | Symbol | I/O |  |
| :---: | :---: | :---: | :--- |
| $1 \sim 22$ | S22~S1 | O | FL Segment control signal |
| 23 | VPP | - | Power supply terminal |
| $24 \sim 39$ | G15~G1/KO0~5 | O | FL grid control signal / Key matrix output |
| 40,41 | JOG1,2 | I | Source select JOG1,2 |
| 42,43 | JOG3,4 | I | Volume JOG 3,4 |
| 44 | M BUSY | O | BUSY Signal output to IC401 |
| 45 | M CLK | I/O | Clock signal to IC401 |
| 46 | M COMMAND | I | Command data input from IC401 |
| 47 | M STATUS | O | Status signal output to IC401 |
| 48 | M CS | I | Chip select signal input from IC401 |
| 49 | RM | I | Remote control signal input |
| 50 | VCRI | I | AV Compu-link VCR input |
| 51 | DCSI | I | AV Compu-link DCS input |
| 52 | DCSO | O | AV Compu-link DCS output |
| 53 | VCRO | O | AV Compu-link VCR output |
| 54 | TVD | O | AV Compu-link TV output |
| 55 | TVC | O | AV Compu-link TV control output |
| 56,57 | JOG5,6 | I | Multi JOG 5,6 |
| 58 | POWER | I | Power ON control output |
| 59 |  | O | STANDBY LED control H:Lighting |
| $60 \sim 63$ | KI3~KI0 | I | Key matrix input |
| $64 \sim 67$ | S36~S33 | O | FL Segment control signal |
| 68 | RST | I | Reset input |
| 69 | X1 | - | Connect to GND |
| 70 | X2 | - | Non connect |
| 71 | VSS | - | Connect to GND |
| 72 | OSC2 | - | Oscillation terminal 6MHz |
| 73 | OSC1 | - | Oscillation terminal 6MHz |
| 74 |  | - | Not use |
| $75 \sim 84$ | S32~S23 | O | FL Segment control signal |

## MB90088 (IC203) : On screen display controller

1.Terminal layout

2.Block diagram


## 3.Pin functions (MB90088)

| pin <br> ho | Symbol | I/O | Function |
| :---: | :--- | :--- | :--- |
| 1 | YIN | I | Brightness signal Input terminal for Superinpause indication |
| 2 | VIN | I | Composite video signal input terminal for Superinpause indication |
| 3 | CIN | I | Contrast signal input terminal for Superinpause indication |
| 4 | AVcc | - | Analog power supply terminal |
| 5 | IOUT | O | Color (Brightness) signal output terminal |
| 6 | VOC | O | Character output terminal |
| 7 | Vcc | - | Power supply terminal |
| 8 | EXS | I | Clock generater outside circuit terminal for color burst |
| 9 | XS | O |  |
| 10 | $\overline{\text { HSYNC }}$ | O | Horizontal signal output terminal |
| 11 | $\overline{\text { VSYNC }}$ | O | Vertical signal output terminal |
| 12 | EXHSYN | I | EXT horizontal signal input terminal |
| 13 | EXVSYN | I | EXT vertical signal input terminal |
| 14 | Vss | - | GND |
| 15 | EXD | I | Dot clock generater outside circuit signal terminal for indication |
| 16 | XD | O |  |
| 17 | VOB | O | Character \& background signal output terminal |
| 18 | GOUT | O | Color signal (Green, Red, Blue) |
| 19 | ROUT |  |  |
| 20 | BOUT |  |  |
| 21 | TEST | I | Test signal input terminal |
| 22 | SCLK | I | Shift clock input terminal for serial transmission |
| 23 | SIN | I | Serial data input terminal |
| 24 | CS | I | Chip select terminal |
| 25 | COUT | O | Contrast signal output terminal |
| 26 | VOUT | O | Composite video signal output terminal |
| 27 | YOUT | O | Brightness signal output terminal |
| 28 | AVss | - | Analog GND terminal |
|  |  |  |  |

## ■ NJM2285D (IC202) : Video switch

1.Terminal layout \& Block diagram


## - TC9164AN (IC432): Analog switch

1.Function

Switch to On/Off of S1 to S8 by control of LSI.
2.Terminal Lay out \& Block Diagram


## ■ PQ3DZ53 (IC661, IC663) : Regulator IC



## TC9446F-013(IC631):Digital signal processor for dolby digital

 / DTS audio decode| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | $\overline{\text { RST }}$ | 1 | Reset signal input terminal (L:reset H:Operation usually) |
| 2 | MIMD | 1 | Microcomputer interface mode selection input terminal (L:serial H:IC bus) |
| 3 | $\overline{\text { MICS }}$ | I | Microcomputer interface chip select input terminal |
| 4 | $\overline{\text { MILP }}$ | 1 | Microcomputer interface latch pulse input |
| 5 | MIDIO | 1/0 | Microcomputer interface data l/O terminal |
| 6 | MICK | I | Microcomputer interface clock input terminal |
| 7 | MIACK | 0 | Microcomputer interface acknowledge output terminal |
| 8~11 | FIO~3 | 1 | Flag input terminal 0~3 |
| 12 | IRQ | 1 | Interrupt input terminal |
| 13 | VSS | - | Digital ground terminal |
| 14 | LRCKA | 1 | Audio interface LR clock input terminal A |
| 15 | BCKA | I | Audio interface bit clock input terminal A |
| 16~18 | SDO0~2 | 0 | Audio interface data output terminal 0 |
| 19 | SD03 | - | Non connect |
| 20 | LRCKB | 1 | Audio interface LR clock input terminal B |
| 21 | BCKB | 1 | Audio interface bit clock input terminal B |
| 22 | SDT0 | I | Audio interface data input terminal 0 |
| 23 | SDT1 | 1 | Audio interface data input terminal 1 |
| 24 | VDD | - | Power supply for digital circuit |
| 25 | LRCKOA | 0 | Audio interface LR clock output terminal A |
| 26 | BCKOA | 0 | Audio interface bit clock output terminal A |
| 27,28 | TEST0,1 | 1 | Test input terminal 0/1 (L:test H:operation usually) |
| 29~31 | LRCKOB,BCKOB,TXO | - | Non connect |
| 32,33 | TEST2,3 | I | Test input terminal (L:test H:operation usually) |
| 34 | RX | 1 | SPDIF input terminal |
| 35 | VSS | - | Ground terminal for digital circuit |
| 36 | TSTSUB0 | 1 | Test sub input terminal 0 (L:test H:operation usually) |
| 37 | FCONT | 0 | VCO Frequency control output terminal |
| 38,39 | TSTSUB1,TSTSUB2 | 1 | Test sub input terminal 1,2 (L:test H:operation usually) |
| 40 | PDO | 0 | Phase error signal output terminal |
| 41 | VDDA | - | Power supply for analog circuit |
| 42 | PLON | 1 | Clock selection input terminal (L:external clock H:VCO clock) |
| 43 | AMPI | 1 | AMP.input terminal for LPF |
| 44 | AMPO | 0 | AMP.output terminal for LPF |
| 45 | CKI | 1 | External clock input terminal |
| 46 | VSSA | - | Ground terminal for analog circuit |
| 47 | CKO | 0 | DIR Clock output terminal |
| 48 | LOCK | 0 | VCO Lock detection output terminal |
| 49 | VSS | - | Ground terminal for digital circuit |
| 50 | WR | 0 | External SRAM writing signal output terminal |
| 51 | OE | 0 | External SRAM output enable signal output terminal |
| 52 | $\overline{\mathrm{CE}}$ | 0 | External SRAM chip enable signal output terminal |
| 53 | VDD | - | Power supply terminal for digital circuit |
| 54~61 | 107~0 | I/O | External SRAM data I/O terminal 7~0 |
| 62 | VSS | - | Ground terminal for digital circuit |
| 63~70 | AD0~7 | 0 | External SRAM address output terminal 0~7 |
| 71 | VDD | - | Power supply terminal for digital circuit |
| 72~80 | AD8~16 | 0 | External SRAM address output terminal 8~16 |
| 81 | VSS | - | Ground terminal for digital circuit |
| 82~89 | POO~7 | 0 | General purpose output terminal 0~7 |
| 90 | VDDDL | - | Power supply terminal for DLL |
| 91 | LPFO | 0 | LPF output terminal for DLL |
| 92,93 | DLON,DLCKS | 1 | Refer to the undermentioned table |
| 94 | SCKO | - | Non connect |
| 95 | VSSDL | - | Ground terminal for DLL |
| 96 | SCKI | 1 | External system clock input terminal |
| 97 | VSSX | - | Ground termonal for oscillation circuit |
| 98,99 | XO, XI | I/O | Oscillation I/O terminal |
| 100 | VDDX | - | Power supply terminal for oscillation circuit |


| DLCKS terminal | DLONterminal | DLL clock setting |
| :---: | :---: | :--- |
| L | L | SCKI input (DLL circuit OFF) |
| L | H | Four times XI clock |
| H | L | Three times XI clock |
| H | H | Six times XI clock |

TC9459F (IC331,IC332,IC333) : Electronic volume control
1.Pin layout

2. Block diagram


## 3.Pin function

| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
| :---: | :--- | :--- | :--- | :--- | :--- |
| 1 | VSS | Negative power supply pin | 13 | DATA | Volume setup serial data input |
| 2 | L-OUT | Volume output pin | 14 | STB | Data write strobe input |
| 3 | NC | No connection | 15 | NC | No connection |
| 4 | NC | No connection | 16 | CS2 | Chip select input pin |
| 5 | L-LD1 | Loudness tap output pin | 17 | NC | No connection |
| 6 | L-LD2 | Loudness tap output pin | 18 | R-A-GND | Analog GND pin |
| 7 | L-A-GND | Analog GND pin | 19 | R-LD2 | Loudness tap output pin |
| 8 | NC | No connection | 20 | R-LD1 | Loudness tap output pin |
| 9 | CS1 | Chip select input pin | 21 | R-IN | Volume input pin |
| 10 | NC | No connection | 22 | NC | No connection |
| 11 | NC | No connection | 23 | R-OUT | Volume output pin |
| 12 | CK | Data transfer clock input | 24 | VDD | Positive power supply pin |

## U UPD78F4216AGC(IC671):UNIT CPU

1. Pin layout

| 75 | $\sim$ | 51 |  |  |
| :---: | :---: | :---: | :---: | :---: |
| 76 |  |  |  | 50 |
| 2 |  |  |  | 2 |
| 100 |  |  |  | 26 |
|  | 1 | $\sim$ | 25 |  |

## 2.Pin function

| Pin No. | Symbol | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1~8 |  | - | Non connect |
| 9 | VDD | - | Power supply terminal |
| 10 | X2 | 0 | Connecting the crystal oscillator for system main clock |
| 11 | X1 | 1 | Connecting the crystal oscillator for system main clock |
| 12 | VSS | - | Connect to GND |
| 13 | XT2 | 0 | Connecting the crystal oscillator for system sub clock |
| 14 | XT1 | 1 | Connecting the crystal oscillator for system sub clock |
| 15 | RESET | 1 | System reset signal input |
| 16 | AUTODATA | 1 | Output of DSP to general-purpose port |
| 17 | LOCK | 1 | Output of DSP to general-purpose port |
| 18 | DIGITALO | 1 | Output of DSP to general-purpose port |
| 19 | FORMAT | 1 | Output of DSP to general-purpose port |
| 20 | CHANNEL | 1 | Output of DSP to general-purpose port |
| 21 | ERR | 1 | Output of DSP to general-purpose port |
| 22 | RSTDET | 1 | Reset signal input |
| 23 | AVDD | - | Power supply terminal |
| 24 | AVREF0 | - | Connect to GND |
| 25~32 |  | - | Connect to GND |
| 33 | AVSS | - | Connect to GND |
| 34,35 |  | - | Non connect |
| 36 |  | - | Power supply terminal |
| 37,38 | RX,TX | - | Not use |
| 39 |  | - | Non connect |
| 40 | DSPCOM | 1 | Communication port from IC401 |
| 41 | DSPSTS | 0 | Status communication port to IC401 |
| 42 | DSPCLK | 1 | Clock input from IC401 |
| 43 | DSPRDY | 1 | Ready signal input from IC401 |
| 44 |  | - | Non connect |
| 45,46 | MIDIO IN/OUT | I/O | Interface I/O terminal with microcomputer |
| 47 | $\overline{\mathrm{MICK}}$ | 0 | Interface I/O terminal with microcomputer of clock signal |
| 48 | MICS | 0 | Interface I/O terminal with microcomputer of chip select |
| 49 | MILP | 0 | Interface I/O termonal with microcomputer |
| 50 | $\overline{\text { MIACK }}$ | 0 | Interface I/O termonal with microcomputer |
| 51,52 |  | - | Non connect |
| 53 | $\overline{\text { DSPRST }}$ | 0 | Reset signal output of DSP |
| 54~63 |  | - | Non connect |
| 64,65 | CDTI/CDTO | I/O | Interface I/O terminal with microcomputer |
| 66 | $\overline{\text { CCLK }}$ | 0 | Interface I/O terminal with microcomputer of clock signal |
| 67 | $\overline{\text { CS }}$ | 0 | Interface I/O terminal with microcomputer of chip select |
| 68 | XTS | 0 | OSC Select |
| 69,70 |  | - | Non connect |
| 71 | $\overline{\text { PD }}$ | 0 | Reset signal output |
| 72 | GND | - | Connect to GND |
| 73~80 |  | - | Non connect |
| 81 | VDD | - | Power supply |
| 82 | 3D-ON | - | Non connect |
| 83 | 3D-ON | 0 | Switch at output destination of surround channel |
| 84 | ANA/T-TONE | 0 | Test tone control |
| 85 | REF-MIX | 0 | Control at output destination of LFE channel |
| 86 |  | - | Non connect |
| 87 | D.MUTE | 0 | Mute of the digital out terminal is controlled |
| 88 | S.MUTE | 0 | Mute of the audio signal is controlled |
| 89 |  | - | Non connect |
| 90~93 | ASW1~4 | 0 | Selection of digital input selector |
| 94 | TEST | - | Test terminal |
| 95~100 |  | - | Non connect |

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